AMENDMENTS TO THE DRAWINGS:

The attached replacement sheet of drawings includes changes to Fig. 6. The replacement sheet, which includes original Figs. 3-5 and amended FIG. 6, replaces the original sheet including Figs. 3-6.

In Fig. 6, original reference numeral "60" has been replaced with --66--.

Attachment:

- Replacement Sheet

REMARKS

Applicants appreciate the Examiner's thorough review of the present application, and respectfully request reconsideration in light of the preceding amendments and the following remarks.

Claims 1-17 and 22-25 are pending in the application. The non-elected claims 16-21 have been canceled. Claim 1 has been amended to better define the claimed invention. Claims 22-25, readable on the elected species/invention, have been added to provide Applicants with the scope of protection to which they are believed entitled. The amended/added claims find solid support in the original specification, e.g., at page 4, lines 27-29, and the original drawings, e.g., FIGs. 1 and 3-6. The Abstract and FIG. 6 have been revised to remove certain informalities. No new matter has been introduced through the foregoing amendments.

The drawing objection is believed overcome in view of the amendment made to FIG. 6 in the manner kindly suggested by the Examiner in paragraph 3 of the Office Action.

35 U.S.C. 102(e) rejection of claims 1-6, 10, 14 and 15 as being anticipated by *Van Horn et al.* (USPN-6,563,299)

Regarding Claim 1

Amended claim 1 recites an **impedance standard substrate for calibrating a vector network analyzer,** said vector network analyzer including two probes, said impedance standard substrate comprising: a first surface; a second surface opposite to the first surface; and a thru-circuit having two contacts electrically connected to each other and respectively disposed on the first surface and the second surface, wherein **the contacts are adapted electrically connect to the two probes of the vector network analyzer, respectively**.

The invention of claim 1 finds solid support in the application as filed. In particular, as shown in FIGs. 1 and 2d, **the impedance standard substrate 30 is adapted to calibrate the vector network analyzer 10 including two probes 22, 23**. Furthermore, as shown in FIGs. 1, 2d and 3-6, the thru-circuit 50 has **two contacts 52, 54 adapted to contact two probes 22, 23 of the vector network analyzer 10**. On page 6, lines 24-27 of specification, it is further disclosed that the vector network analyzer can use **the impedance standard substrate** to obtain **two-side calibration data** so as to directly measure **the device under test (DUT) with two-side contacts**. Therefore, the vector network analyzer is not required to turn the probe by means of complex mechanisms and the calibration data measured is comparatively correct.

Van Horn et al. does not disclose, teach or suggest the claimed invention. Specifically, in column 1, lines 43-46 and FIG. 2, *Van Horn et al.* disclose that a conventional BGA package 100 which is a device under test (DUT) and includes a semiconductor die 110 secured to a die-attach pad 112 formed on an upper surface 106 of a **substrate 105**, which may also be termed an interposer. Thus, *Van Horn et al.* only disclose that **the substrate 105 is a part of the BGA package 100 for supporting the semiconductor die 110 and the die-attach pad 112**. *Van Horn et al.* fail to disclose **a substrate for calibrating a vector network analyzer**. Evidently, **the function of the substrate 105** disclosed by *Van Horn et al.* is distinctly different from **the claimed function of the impedance standard substrate**.

The substrate 105 disclosed by *Van Horn et al.* should be **tested** by a vector network analyzer, but **the claimed impedance standard substrate** is adapted to **calibrate** the vector network analyzer. Evidently, the configuration and purpose of **the substrate 105** disclosed by *Van Horn et al.* are distinctly different from those of **the claimed impedance standard substrate**.

Furthermore, *MPEP*, Section 2111.02 states, "[a]ny terminology in the preamble that limits the structure of the claimed invention must be treated as a claim limitation". The "impedance

standard substrate" recited in the preamble of claim 1 clearly limits the claimed invention to a device configured to calibrate the vector network analyzer and must be treated as a claim limitation. *Van Horn et al.* simply disclose a DUT which is not configured to calibrate any vector network analyzer. The reference therefore fails to render claim 1 unpatentable.

It should be now clear that the Examiner has mischaracterized **the substrate 105** disclosed by *Van Horn et al.* as **the claimed impedance standard substrate**.

In addition, as shown in FIG. 2 of the cited reference, *Van Horn et al.* disclose that the semiconductor die 110 and **the electrical lead 130** are typically encased by an encapsulant material 120. Thus, **the electrical lead 130 cannot directly contact an external device, e.g. a vector network analyzer**. Evidently, **the electrical lead 130** disclosed by *Van Horn et al.* is distinctly different from **the claimed contacts** (e.g., 52, 54).

Accordingly, claim 1 is not anticipated by *Van Horn et al.* and is clearly patentable over *Van Horn et al.*

Regarding Claim 10:

Claim 10 is considered patentable at least for the similar reason advanced with respect to Claim 1.

Regarding Claim 5:

Claim 5 recites the impedance standard substrate further comprising a side wall defined between the first surface and the second surface, wherein the two contacts of the thru-circuit abut the edge of the impedance standard substrate and the thru-circuit further comprises a trace disposed on the **side wall** for electrically connecting the two contacts. The claimed invention finds support in FIG. 5, i.e., the thru-circuit 50 further comprises a trace 64 disposed on the **side**

wall of the impedance standard substrate 30. However, *Van Horn et al.* only disclose that each electrical lead 130 further comprises **a conductive via 134** extending from the conductive pad 133 and **through** the substrate 105 to a conductive trace 136, as shown in FIG. 2. *Van Horn et al.* fail to disclose that **the thru-circuit further comprises a trace disposed on the side wall of the impedance standard substrate**. Evidently, **the claimed thru-circuit** is distinctly different from **the conductive via 134 in substrate 105** disclosed by *Van Horn et al.*

Accordingly, claim 5 is not anticipated by *Van Horn et al.* and is clearly patentable over *Van Horn et al.*

Regarding Claims 2-4 and 6:

Claims 2-4 and 6 depend from claim 1, and are considered patentable at least for the reasons advanced with respect to claim 1.

Regarding Claims 14 and 15:

Claims 14 and 15 depend from claim 10, and are considered patentable at least for the reasons advanced with respect to claim 10.

35 U.S.C. 103(a) rejection of claims 7-9 and 11-13 as being unpatentable over *Van Horn et al.* (USPN-6,563,299) in view of *Dunsmore* (USPN-6,643,597).

MPEP, Section 2143 states, "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, **there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings**. Second, **there must be a reasonable expectation of success**. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

Applicants respectfully submit that the references cannot be properly combined for the following reasons.

Van Horn et al. only disclose that **the substrate 105** is a part of the BGA package 100 for supporting the semiconductor die 110 and the die-attach pad 112 (as shown in FIG. 2), and *Dunsmore* only disclose **a short model 230, a open model 240 and a load model 250** according to the method for calibrating a test system (as disclosed in column 8 line 41 to column 9 line 2, column 10, lines 26-58, column 10, line 59 to column 11, line 29, and column 11, lines 30-56). Thus, there is no suggestion or motivation to combine the teachings of *Van Horn et al.* and *Dunsmore*, contrary to the Examiner's allegation. Second, there is no reasonable expectation of success upon combining the teachings of *Van Horn et al.* and *Dunsmore.*

Evidently, the Examiner impermissibly relied on hindsight to combine the teachings of *Van Horn et al.* and *Dunsmore* to arrive at claims 7-9 and 11-13.

Finally, *Dunsmore* is non-analogous art that is neither in the field of applicant's endeavor nor reasonably pertinent to the particular problem with which the inventor was concerned. *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992). *See* also *In re Deminski*, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986); *In re Clay*, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992). *See* also *MPEP*, section 2141.01(a). It is sufficient to note the classifications of *Dunsmore* (**702**/104) and *Van Horn et al.* (**324**/158) to recognize how remote *Dunsmore* is from the field of the claimed invention.

Accordingly, claims 7-9 and 11-13 are not obvious over the applied references of *Van Horn et al.* and *Dunsmore.*

Regarding Claims 7-9:

Claims 7-9 depend from Claim 1, and are considered patentable at least for the reasons advanced with respect to claim 1.

Regarding Claims 11-13:

Claims 11-13 depend from Claim 10, and are considered patentable at least for the reasons advanced with respect to claim 10.

Regarding Claims 22-25:

Claims 22-25 depend from claim 1 or 10, and are considered patentable at least for the reasons advanced with respect to amended claim 1 and 10. Claims 22-25 are also patentable on their own merits since these claims recite other features of the invention neither disclosed, taught nor suggested by the applied art.

As to claim 22, the applied references, especially *Van Horn et al.*, clearly fail to disclose, teach or suggest **two exposed contacts** on the first and second surfaces, respectively. As can be seen in FIG. 2 of *Van Horn et al.*, one of the "contacts," i.e., 130, is buried in the encapsulating material 120 and cannot be regarded as being exposed.

As to claim 23, the applied references, especially *Van Horn et al.*, clearly fail to disclose, teach or suggest that each of the two probes of the vector network analyzer is brought in **direct, electrical and physical contact** with one of the two contacts of the substrate. Again, note FIG. 2 of *Van Horn et al.* where one of the "contacts," i.e., 130, is disclosed to be buried in the encapsulating material 120 and cannot come in any direct contact with a probe.

As to claim 24, the applied references, especially *Van Horn et al.*, clearly fail to disclose, teach or suggest **two exposed contacts** as argued with respect to claim 22.

As to claim 25, the applied references, especially *Van Horn et al.*, clearly fail to disclose, teach or suggest that the two probes of the vector network analyzer are **simultaneously** brought in direct, electrical and physical contact with the respective two contacts of the substrate. Again, note FIG. 2 of *Van Horn et al.* where one of the "contacts," i.e., 130, is disclosed to be buried in the encapsulating material 120 and cannot come in any contact with a probe simultaneously with the other contact, i.e., 132.

Each of the Examiner's rejections has been traversed. Accordingly, Applicants respectfully submit that all claims are now in condition for allowance. Early and favorable indication of allowance is courteously solicited.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

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